AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

Claims 1-10 (canceled).

11. (Original): The fabrication method of claim 1, wherein the forming the buried impurity diffusion regions comprises:

implanting impurity ions at a low concentration into the entire surface of the resultant structure using the conductive layer patterns as a mask so as to form low-concentration buried impurity diffusion regions which are self-aligned with the conductive layer patterns;

forming spacers on the sidewalls of the conductive layer patterns and simultaneously removing the gate insulation layer, so as to partially expose the low-concentration buried impurity diffusion regions; and

implanting impurity ions at a high concentration into the entire surface of the resultant structure using the conductive layer patterns and the spacers as a mask, so as to form high-concentration buried impurity diffusion regions in the low-concentration buried impurity diffusion regions.

12. (Original): The fabrication method of claim 11, wherein in the high-concentration impurity implantation, arsenic (As) ions are implanted at an energy of 40 keV to a dose of 5.0E15 ions/cm^2.

13. (Original): The fabrication method of claim 11, further comprising oxidizing the exposed surface of the semiconductor substrate so as to form grown insulation layers on the surface of the high-concentration buried impurity diffusion regions, after the formation of the high-concentration buried impurity diffusion regions.

14. (Original): The fabrication method of claim 13, wherein the grown insulation layers are formed to a thickness of about 100-1000 Å.

15. (Original): The fabrication method of claim 10, wherein the pad conductive layers are formed of a material capable of forming the ohmic contacts with the word lines.

16. (Original): The fabrication method of claim 15, wherein the pad conductive layers are formed of polysilicon, and the word lines are formed of a polycide layer in which a polysilicon layer and a metal silicide layer are stacked.

17. (Original): The fabrication method of claim 10, after the forming the word lines and the pad conductive layers, further comprising:

forming insulation spacers on the sidewalls of the word lines and pad conductive layers, and

forming cell isolation impurity layers near the surface of the semiconductor substrate where neither the buried impurity diffusion regions nor the word lines are formed.

18. (Original): A method of fabricating a mask read only memory (ROM), comprising:

forming a gate insulation layer on a semiconductor substrate;

forming a first polysilicon layer on the gate insulation layer;

forming photoresist patterns on the first polysilicon layer, which entirely cover a peripheral circuit region but are patterned in a cell array region to expose regions which are to become buried impurity diffusion regions;

performing ion implantation using the photoresist patterns as a mask so as to form buried impurity diffusion regions near the surface of the semiconductor substrate to act as sources/drains of cell transistors and as bit lines, wherein the buried impurity diffusion regions are parallel, separated from each other by a predetermined interval and extend in the same direction;

removing the photoresist patterns, and sequentially stacking a second silicon layer and a metal silicide layer on the first polysilicon layer; and

sequentially etching the first and second polysilicon layers and the metal silicide layer so as to form word lines, wherein the word lines are parallel, separated from each other by a predetermined interval and extend in the perpendicular direction to the buried impurity diffusion regions.

19. (Original): The fabrication method of claim 17, after the second polysilicon layer is formed, further comprising doping the surface of the resultant structure with $POCl_3$ ions so as to provide conductivity to the first and second silicon layers.

20. (Original): The fabrication method of claim 17, wherein the gate insulation layer is formed to a thickness of about 50-150 Å, the first polysilicon layer is formed to a thickness of about 100-1000 Å, the second polysilicon layer is formed to a thickness of about 500-1500 Å, and the metal silicide layer is formed to a thickness of about 500-2000 Å.

21. (Original): A method of fabricating a mask read only memory, comprising:

forming a gate insulation layer over a semiconductor substrate;

forming a first polysilicon layer over the gate insulation layer;

forming photoresist patterns over the first polysilicon layer, which entirely cover a peripheral circuit region but are patterned in a cell array region to expose regions that are to become buried impurity diffusion regions;

performing ion implantation using the photoresist patterns as a mask to form a plurality of buried impurity diffusion regions near the surface of the semiconductor substrate, wherein the buried impurity diffusion regions are formed in parallel, are separated from each other by a first predetermined interval, and extend in the same direction;

removing the photoresist patterns, and sequentially stacking a second silicon layer and a metal silicide layer over the first polysilicon layer; and

sequentially etching the first and second polysilicon layers and the metal silicide layer so as to form a plurality of word lines, wherein the word

lines are formed in parallel, are separated from each other by a second predetermined interval, and extend in a direction perpendicular to that of the buried impurity diffusion regions.

22. (Original): A method of fabricating a mask read only memory, as recited in claim 21, wherein the buried impurity diffusion regions act as bit lines and as sources/drains of cell transistors.

23. (Original): A method of fabricating a mask read only memory, as recited in claim 21, further comprising doping first and second polysilicon layers with $POCl_3$ ions so as to provide conductivity to the first and second polysilicon layers.

24. (Original): A method of fabricating a mask read only memory, as recited in claim 21, wherein the gate insulation layer is formed to a thickness of about 50-150 Å, the first polysilicon layer is formed to a thickness of about 100-1000 Å, the second polysilicon layer is formed to a thickness of about 500-1500 Å, and the metal silicide layer is formed to a thickness of about 500-2000 Å.